I/O contention aware mapping of multi-criticalities real-time applications over many-cores architectures

Laure ABDALLAH (CEA)
Mathieu JAN (CEA)
Jérôme ERMONT (IRIT)
Christian FRABOUl (IRIT)
Many-cores architectures
Motivations

Many-cores architectures

Real-time applications of different level of criticalities
Many-cores architectures

Real-time applications of different level of criticalities

Avionic domain: applications from DAL A to DAL E
Motivations

Many-cores architectures

Real-time applications of different level of criticalities

Processing elements within a backbone Ethernet network
Many-cores architectures

Real-time applications of different level of criticalities

Processing elements within a backbone Ethernet network

TILERA: 3 Ethernet /4 DDR controllers
KALRAY: 8 Ethernet /2 DDR controllers
Many-cores architectures

- Real-time applications of different level of criticalities
- Processing elements within a backbone Ethernet network
- WCTT of flows over Network-on-Chip (NoC) depends on the mapping
Many-cores architectures

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Core-to-Core and Core-to-I/O communications
Many-cores architectures

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Core-to-Core and Core-to-I/O communications
NoC Architecture and Assumptions
Wormhole routing
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Pipeline transmission of packets divided into flow control digits (flits)
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Contentions propagate backwards on the path of flow
NoC Architecture and Assumptions

Wormhole routing

Core-to-I/O flow
NoC Architecture and Assumptions

Wormhole routing

Core-to-I/O flow

Payload divided into NoC packets
NoC Architecture and Assumptions

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Core-to-I/O flow

Payload divided into NoC packets

Transmission into two steps
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Transmission into two steps

All payload received by DDR ➔ frame removed from buffer
Problem illustration

Port labels: port 5, port 4, port 3, port 2, port 1

Nodes labeled: ETH, ETH, ETH
Problem illustration

A state-of-the-art mapping of avionic applications of different size
A state-of-the-art mapping of avionic applications of different size

Critical (DAL A): FADEC

non-critical (DAL E): HM
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2 applications share same ETH interface and each Ethernet frame has a payload of 1500B
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Ethernet 1G
Transmission of HM frame into NoC packets

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HM

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How to integrate the I/O requirements in the mapping?
Existing mapping strategies do not consider the core-to-I/O flows
Contributions

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Our mapping heuristics
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Poster Session