DEMONSTRATION OF THE FMTV 2016 TIMING VERIFICATION CHALLENGE

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Introduction
The FMTV Challenge

- Formal Methods for Timing Verification (FMTV) challenge is to share ideas, experiences and solutions to a concrete timing verification problem issued from real industrial case studies
- Challenge results to be discussed at WATERS (International Workshop on Analysis Tools and Methodologies for Embedded Real-time Systems) 2016 workshop
- https://waters2016.inria.fr/challenge/
- Based on the characteristics of a modern engine management system
- S. Kramer, D. Ziegenbein, and A. Hamann, “Real world automotive benchmark for free,” in Sixth International Workshop on Analysis Tools and Methodologies for Embedded Real-time Systems (WATERS), 2015.
- Model available online:
- http://ecrts.eit.unikl.de/forum/viewtopic.php?f=27&t=62.

Motivation for the Challenge

- Personal observation: risk of divergence between academic research and industrial practice is currently increasing
- Analysis method need to cope with complex mechanisms of modern automotive systems to be meaningful for practical use:
  - mixed preemptive and non-preemptive priority based scheduling
  - periodic, sporadic, and engine synchronous tasks
  - multi-core platform with distributed cause-effect chains including cross-core communication
  - label (i.e. data) placement dependent execution times of runnables
- Many current approaches only address parts of the above mentioned mechanisms
- Can those approaches be extended? Can they (conservatively) approximate the behavior? How tight are the analysis results?

The Challenge
Problem formulation

- Solving the intertwined problem of scheduling including the effects of memory accesses to the execution times is very hard

- Therefore several separate challenges are formulated:
- calculate tight end-to-end latencies ignoring memory accesses and arbitration
- calculate tight end-to-end latencies including memory access and arbitration accesses
- optimize end-to-end latencies by mapping the labels among the local and global memories

The Challenge
HW memory model

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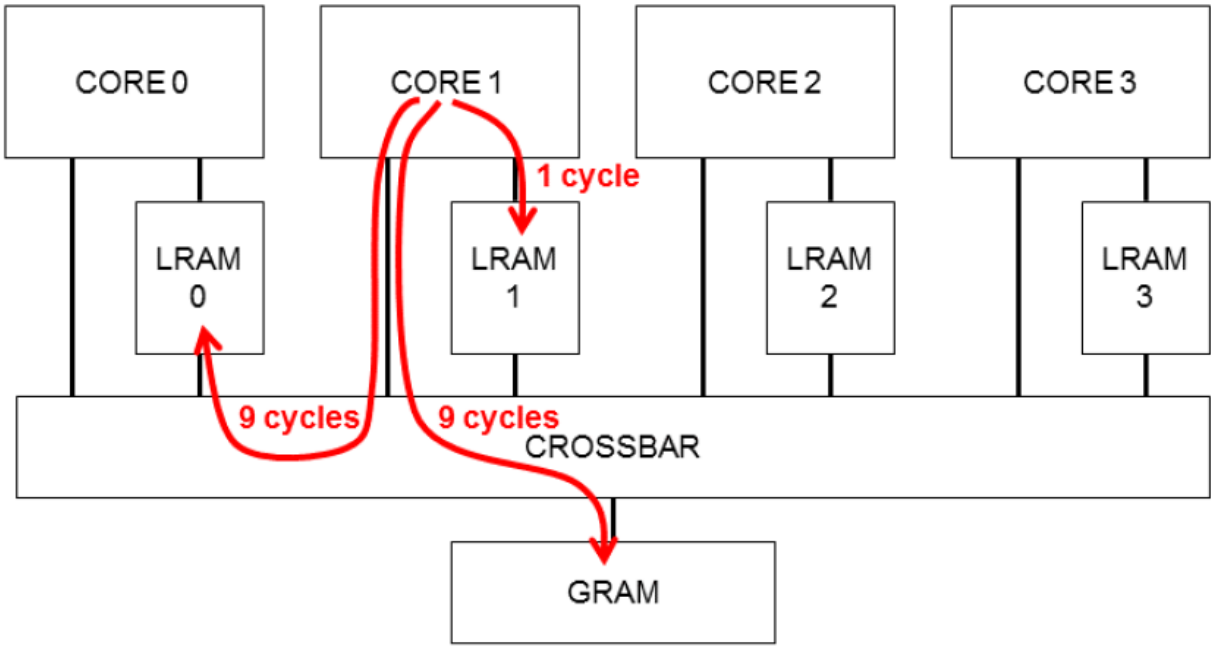
- Access time to data in different memories (local & global)



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The Challenge
SW model

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- Key data of the model
- **1250 Runnables** mapped to
- **21 Tasks & Interrupts** accessing
- **10.000 Labels** (shared data)

- Huge amount of data dependencies challenge exact analysis methods

I	II	III	IV	V	VI
<10	10-50	51-100	100-500	501-1000	>1000

TABLE II. INTER-TASK COMMUNICATION

Period	1 ms	2 ms	5 ms	10 ms	20 ms	50 ms	100 ms	200 ms	1000 ms	sync
1 ms				I	I		I			I
2 ms				I	I		I			
5 ms		I	IV	IV	II	II	I			
10 ms	II	II	II	VI	IV	II	IV	II	III	IV
20 ms	I	I	I	IV	VI	II	IV	I	II	IV
50 ms			II	II	II	III	I			
100 ms		I	I	V	IV	II	VI	II	III	IV
200 ms				I	I		I	I	I	
1000 ms				III	II		III	I	IV	I
Angle-sync	I	I	I	IV	IV	I	III	I	I	V

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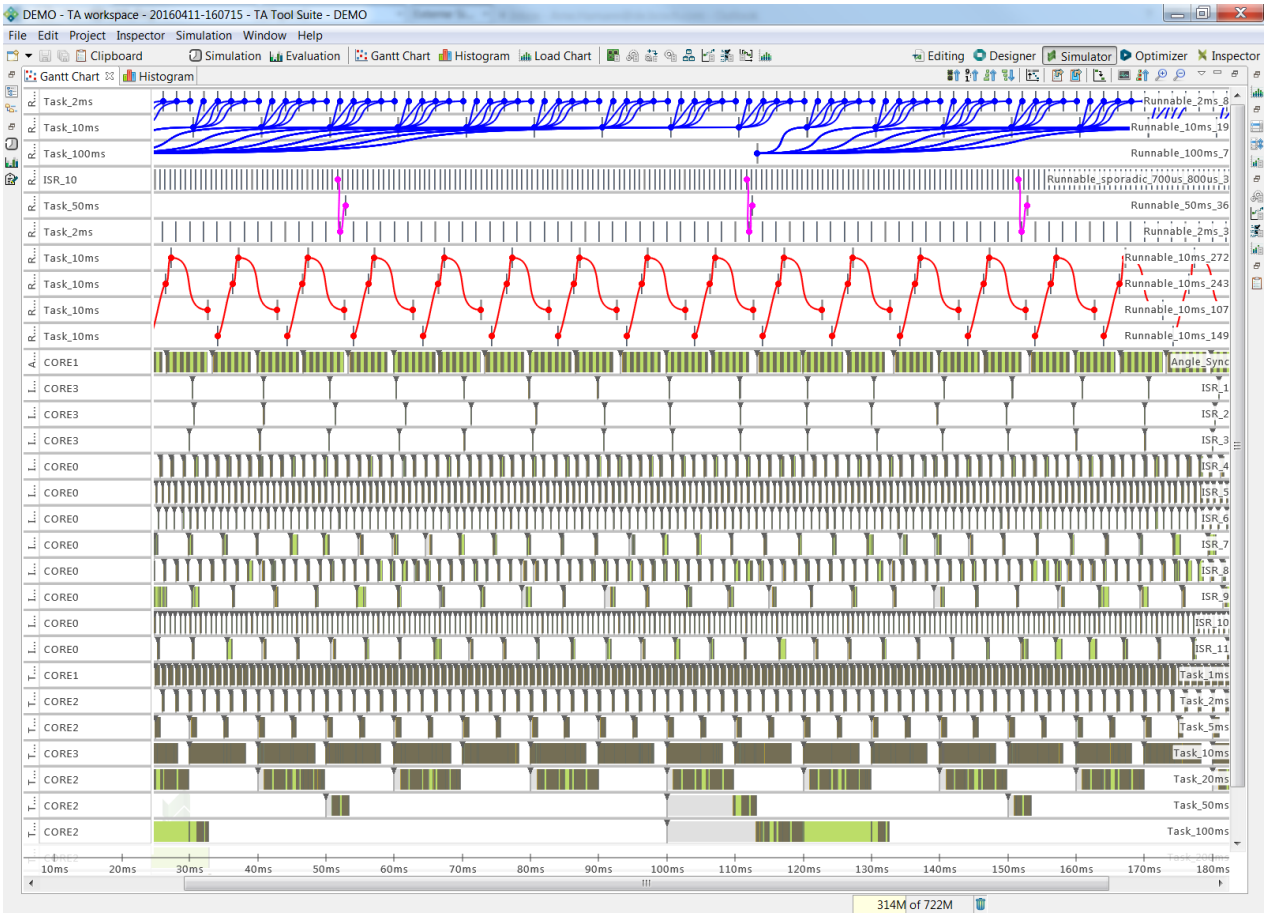
Analysis Results Demo
Scheduling Simulation with TA Tool Suite



Meet us at the demo !

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