

Trading Cores for Memory Bandwidth in Real-time Systems

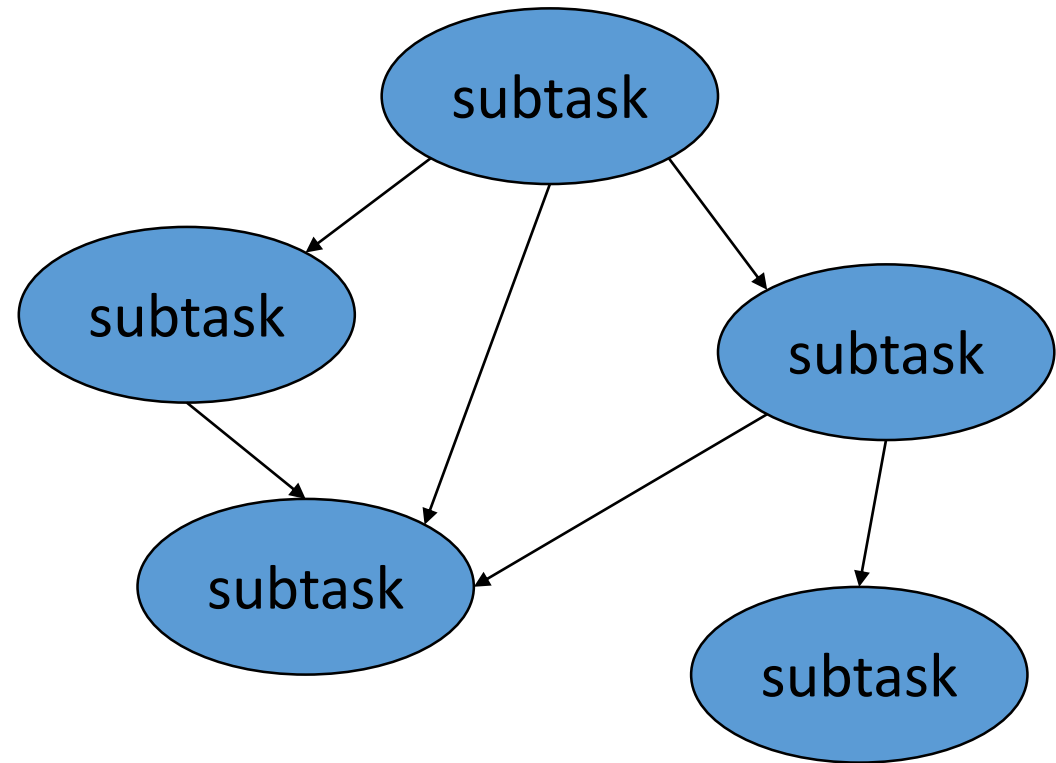
Ahmed Alhammad and Rodolfo Pellizzoni



Outline

- Introduction
- Problem Description
- Our Solution
- Conclusion

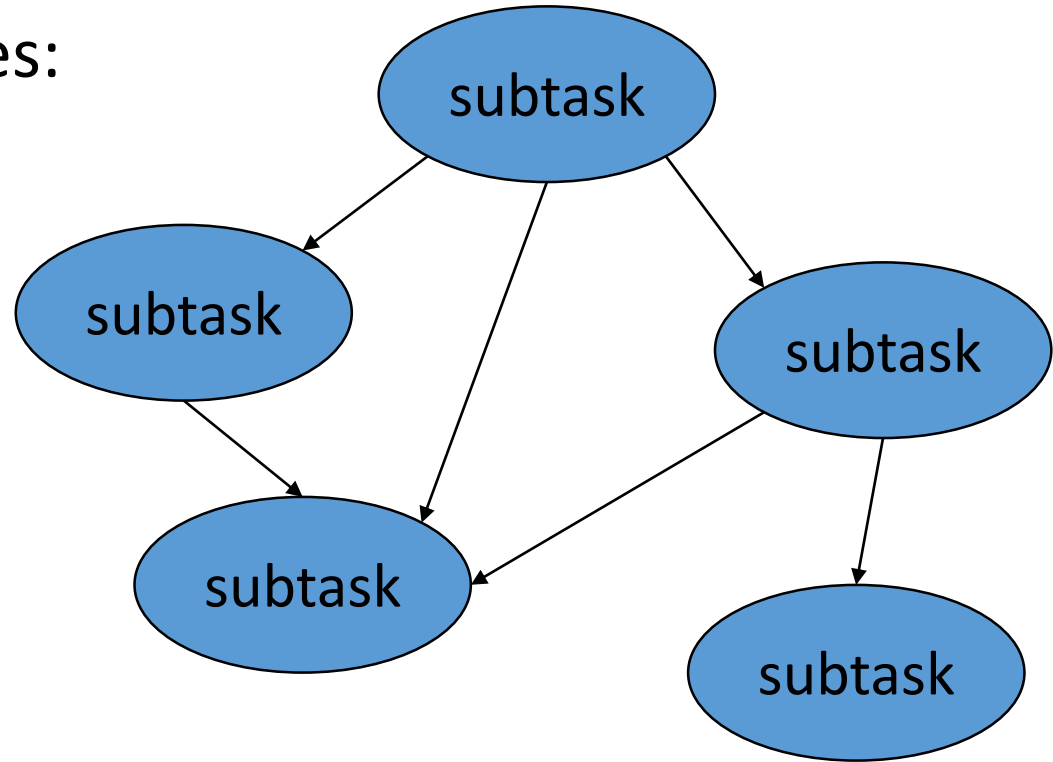
Parallel Tasks



DAG Model

Parallel Tasks

- Two notable scheduling schemes:
 1. Global
 2. Federated



DAG Model

Federated Scheduling

- High utilization tasks ($u_i \geq 1$) are assigned dedicated cores.
- Low utilization tasks ($u_i < 1$) are scheduled as multiprocessor scheduling of sequential tasks.

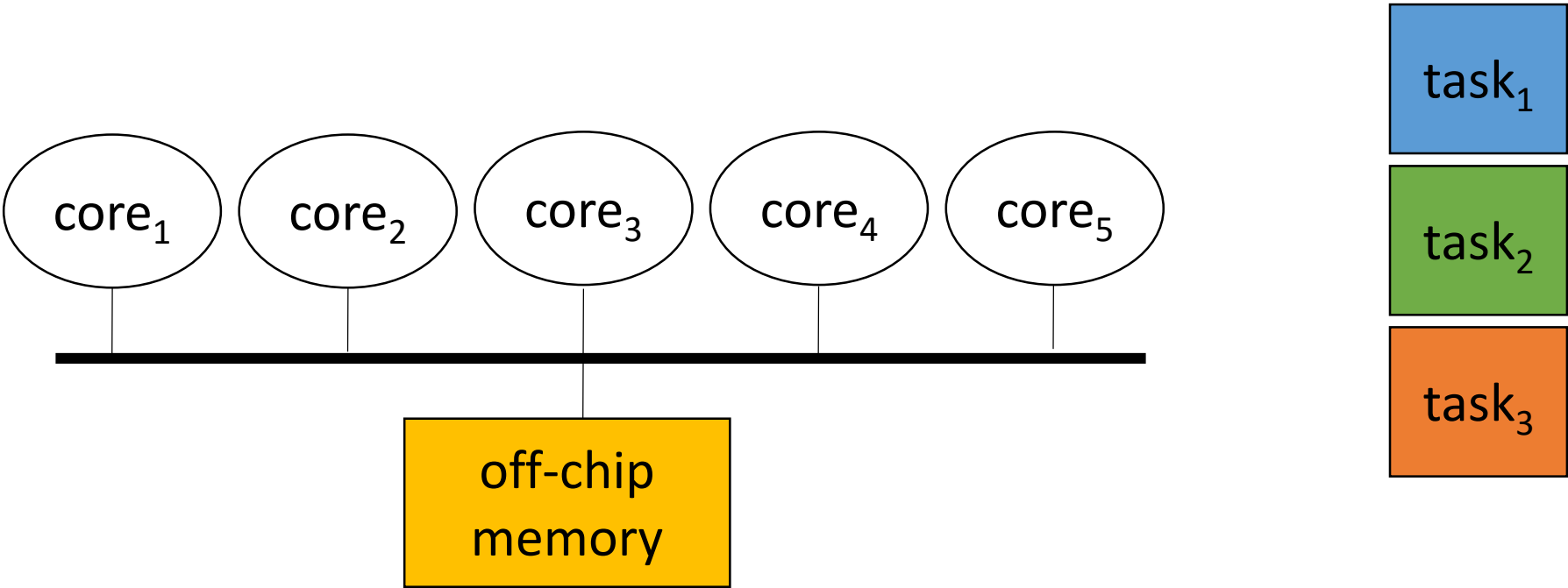
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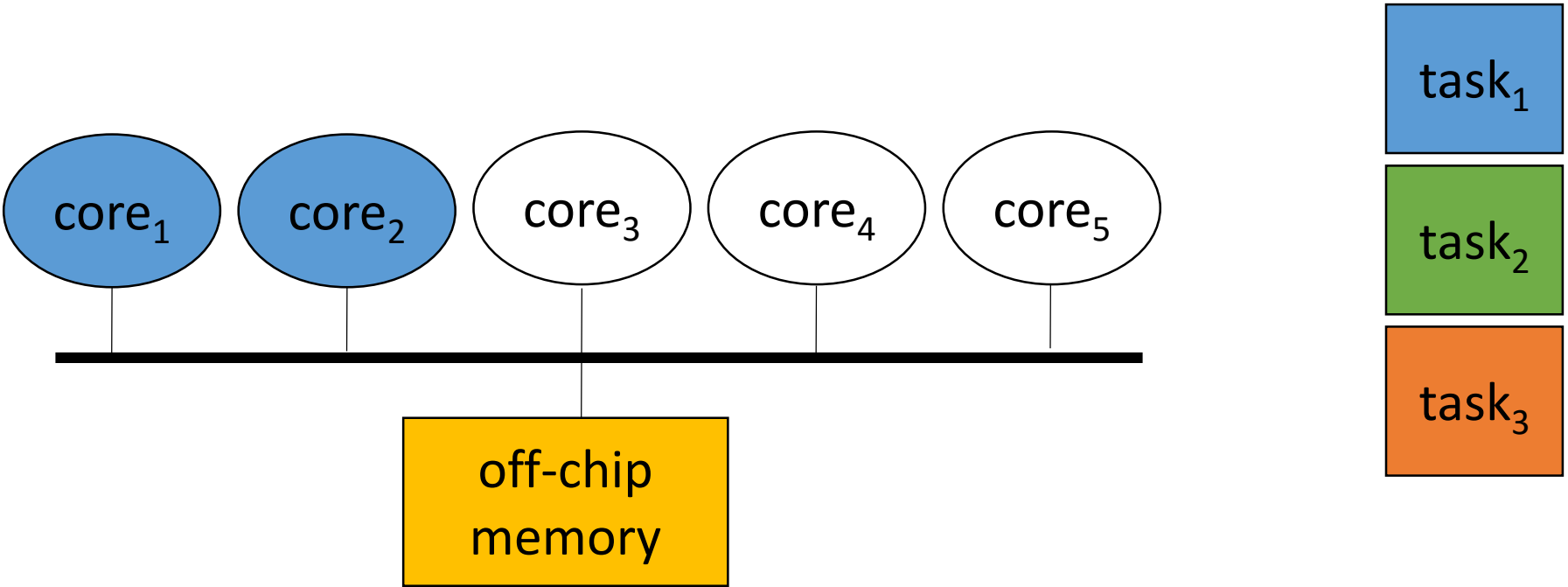
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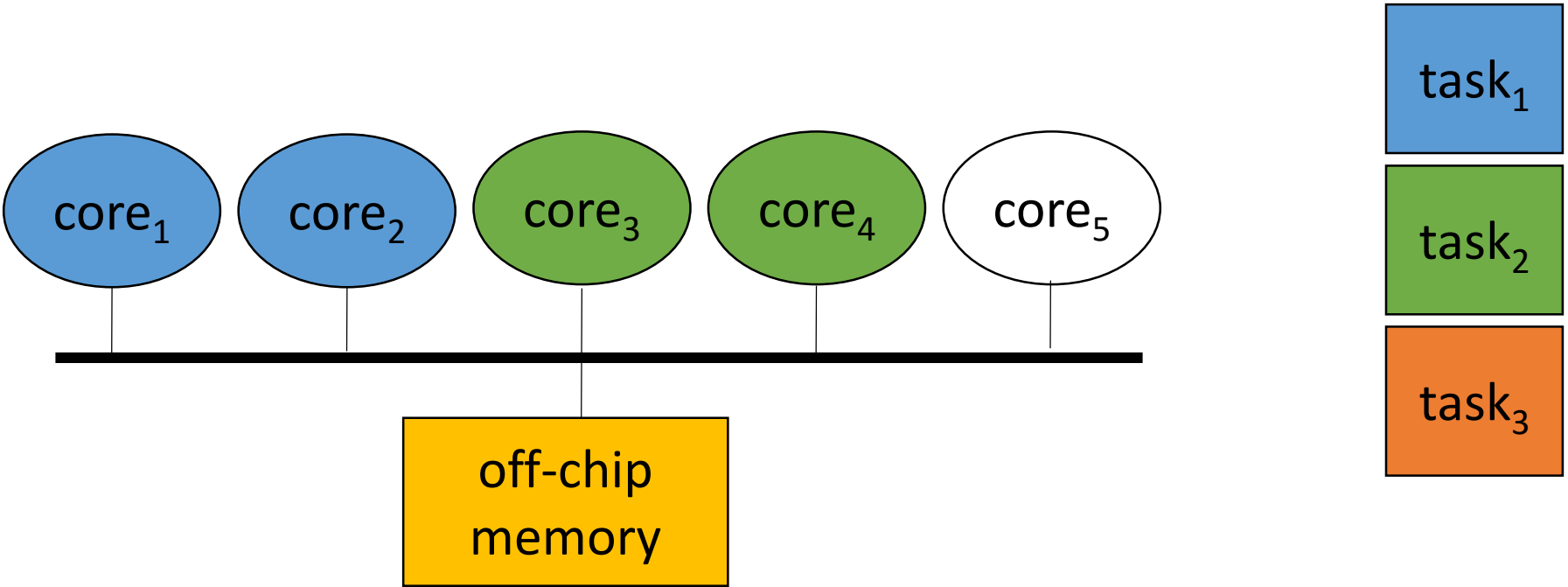
The Problem



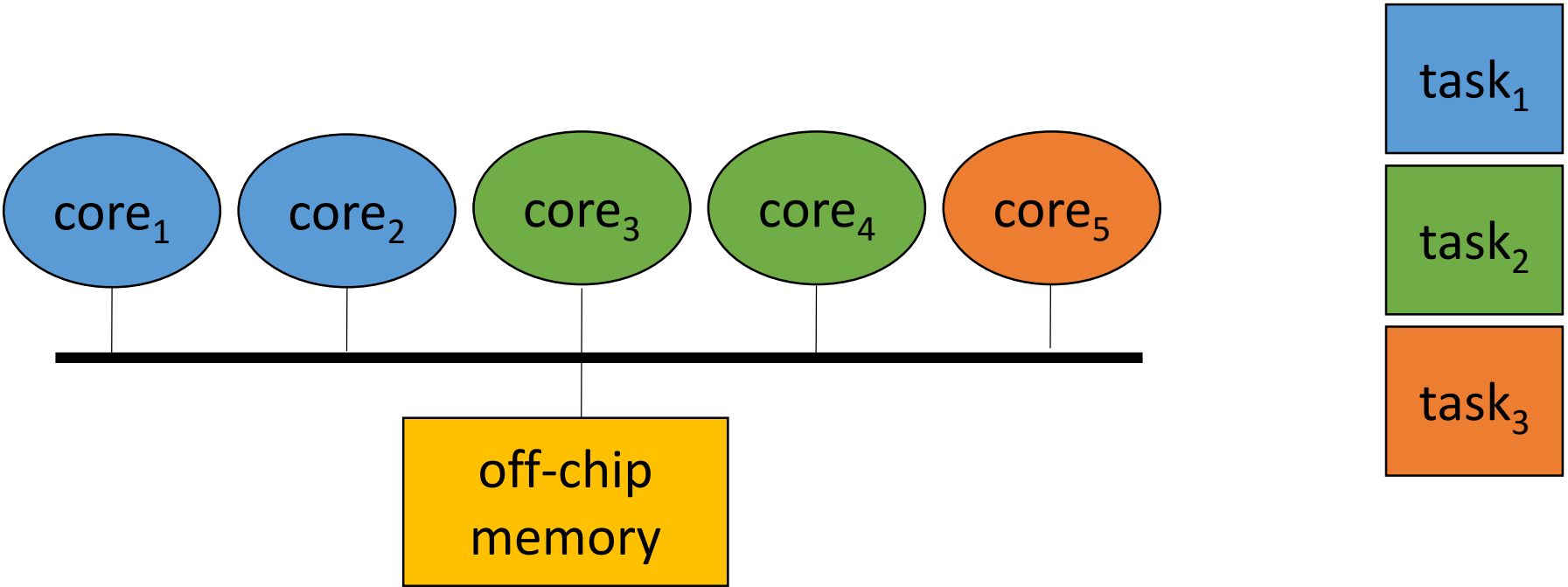
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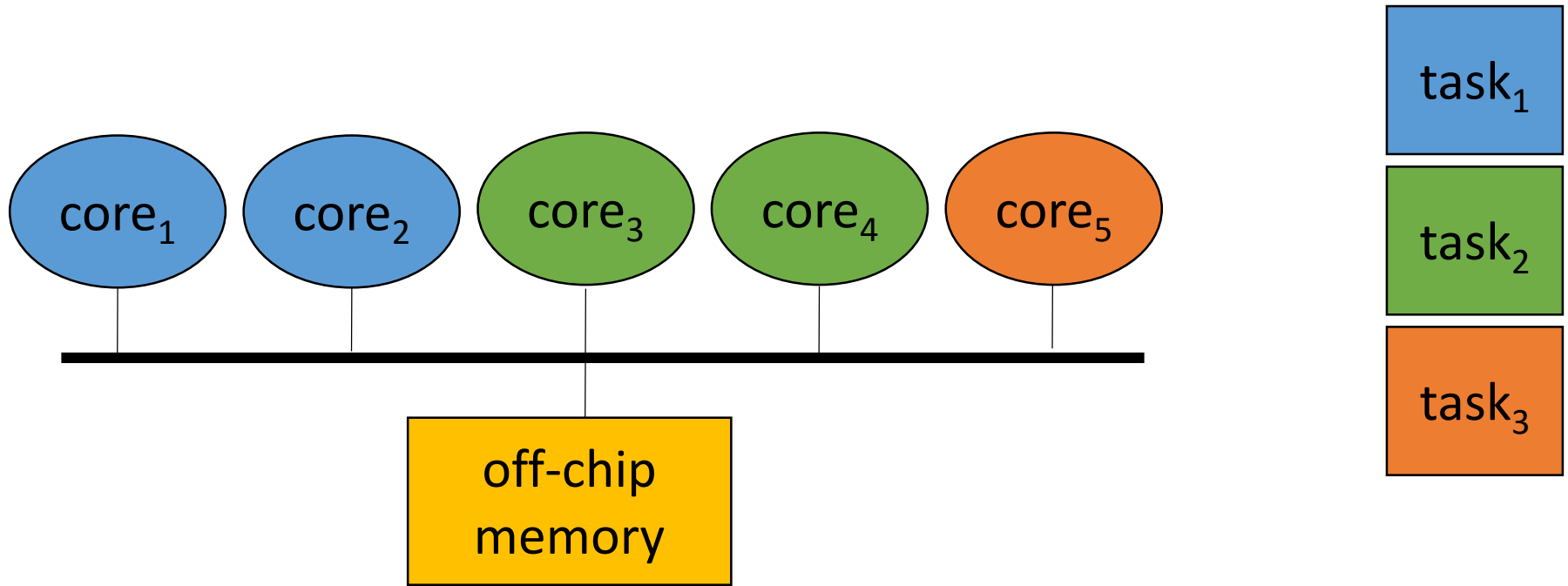
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- Tasks interfere through shared main memory

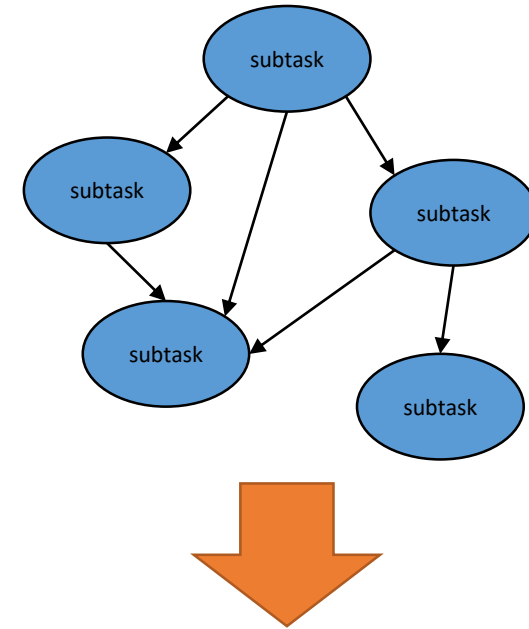
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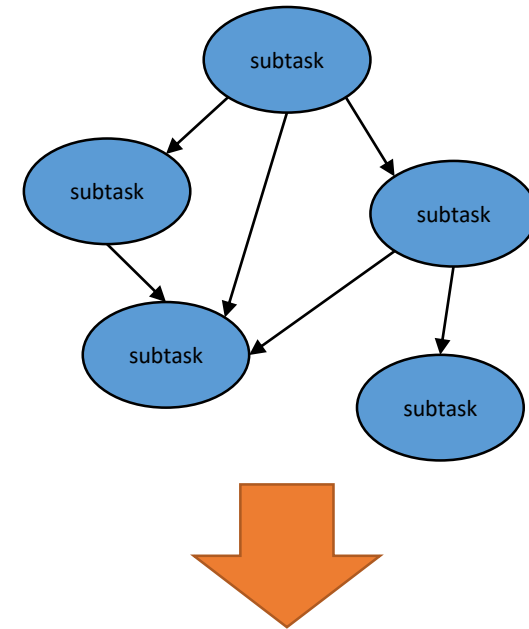
Makespan Bound (greedy scheduling)



m_i number of cores
 q_i bandwidth fraction

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- Each DAG task is characterized by:
 1. Computation volume C_i^e
 2. Memory volume C_i^m
 3. Computation critical path L_i

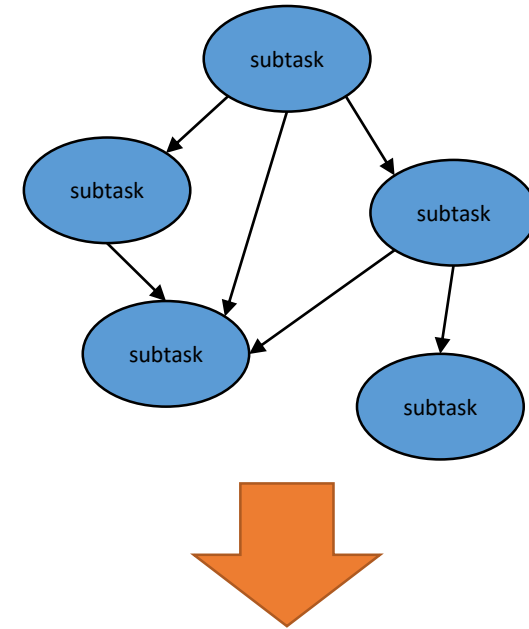


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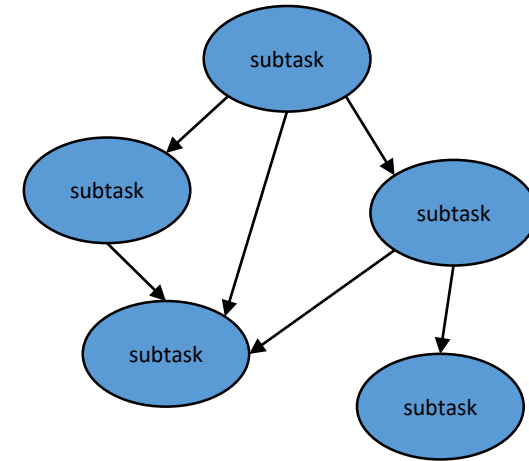
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memory time

computation time



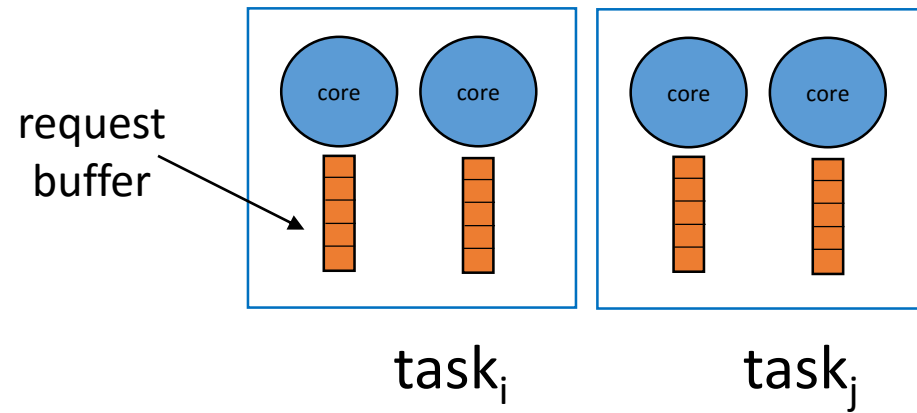
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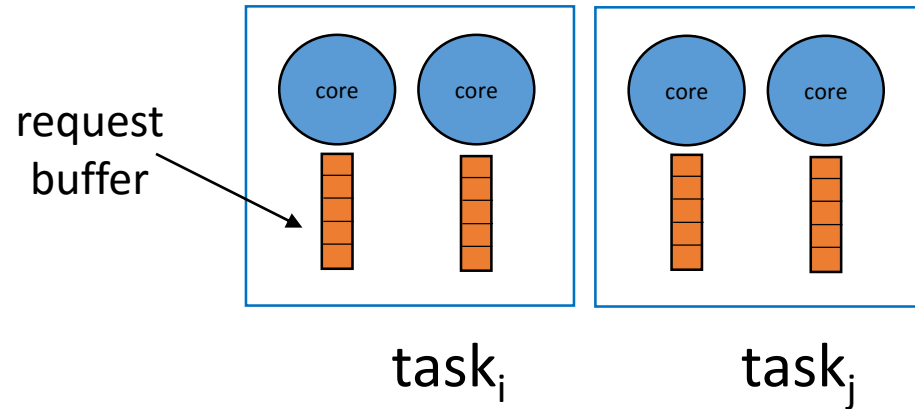
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Round-robin Arbitration

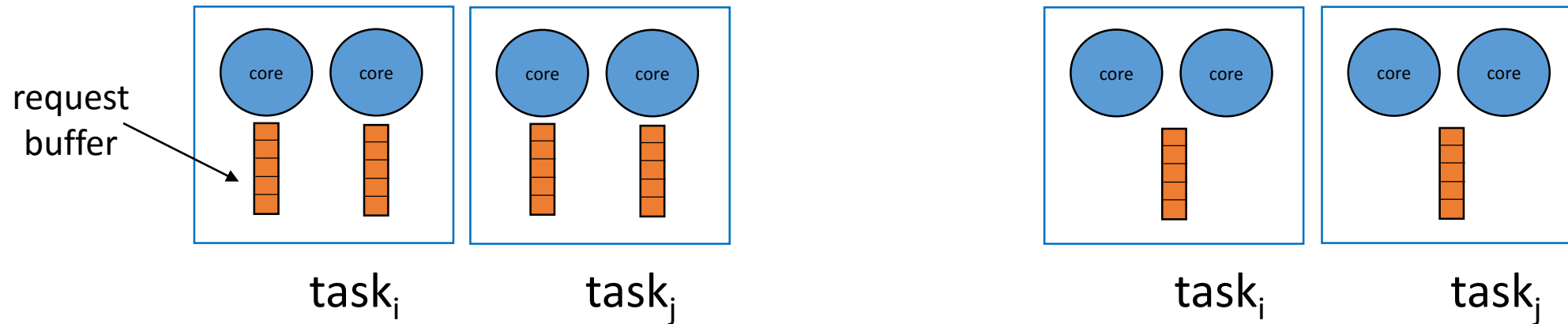


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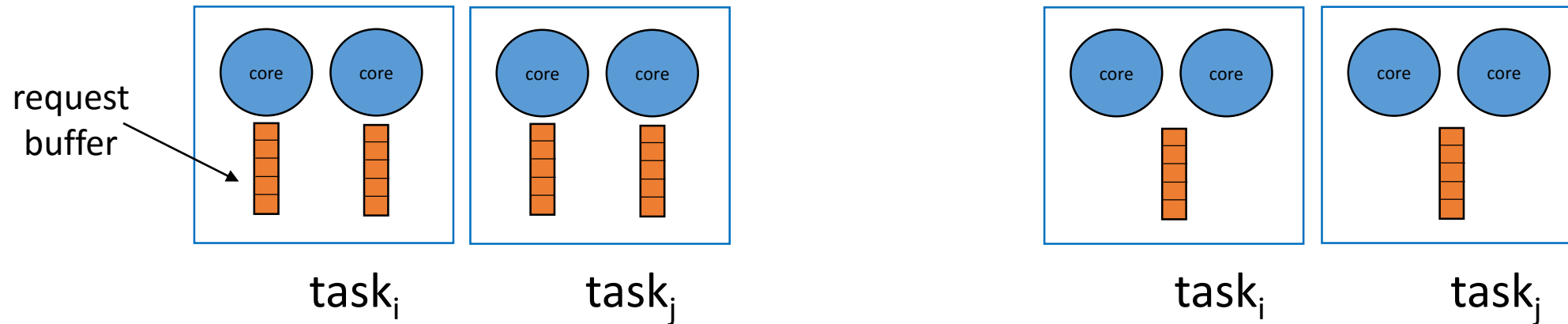
- $C_i^m + C_i^m \times (\sum_{j \neq i} m_j)$

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Round-robin Arbitration



- $C_i^m + C_i^m \times (\sum_{j \neq i} m_j)$

- $C_i^m + C_i^m \times (n - 1)$

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Trading Cores for Memory Bandwidth

- Tasks have different demand regarding memory
- The number of cores is expected to increase
- Memory bandwidth is also growing but in slower rate

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- Memory bandwidth is also growing but in slower rate
- **The idea of trading cores for memory bandwidth**

Example

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 $C_1^m = 50$, $C_1^e = 100$ and $D_1 = 150$

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- The makespan $C_1(\frac{1}{2}, 2) = 50 \times 2 + 100/2 = 150$

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Assignment Algorithm

- Assign each task q_i and m_i such that

$$\sum_{i=1}^n q_i \leq 1 \text{ and } \sum_{i=1}^n m_i \leq m$$

- We propose three algorithms:
 - (1) Optimal algorithm with $q_i \in \mathbb{R}$
 - (2) Harmonic RR with $q_i = 1/2^j$
 - (3) Software-based regulation

Optimal-Assign Algorithm ($q_i \in \mathbb{R}$)

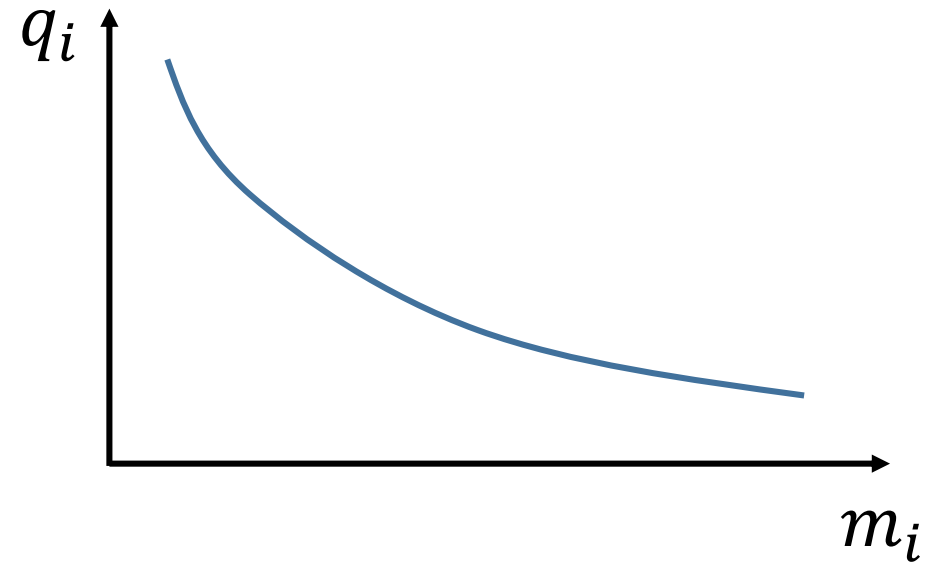
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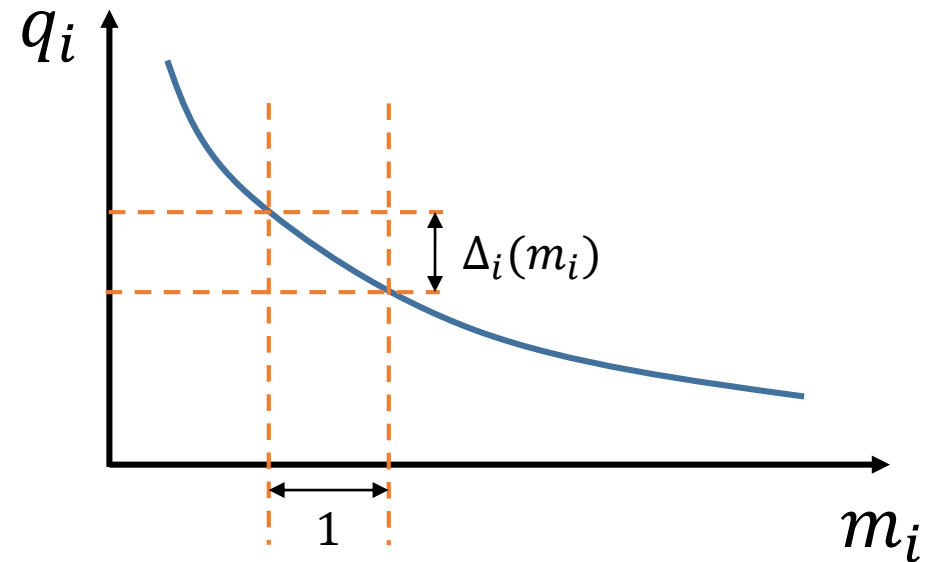
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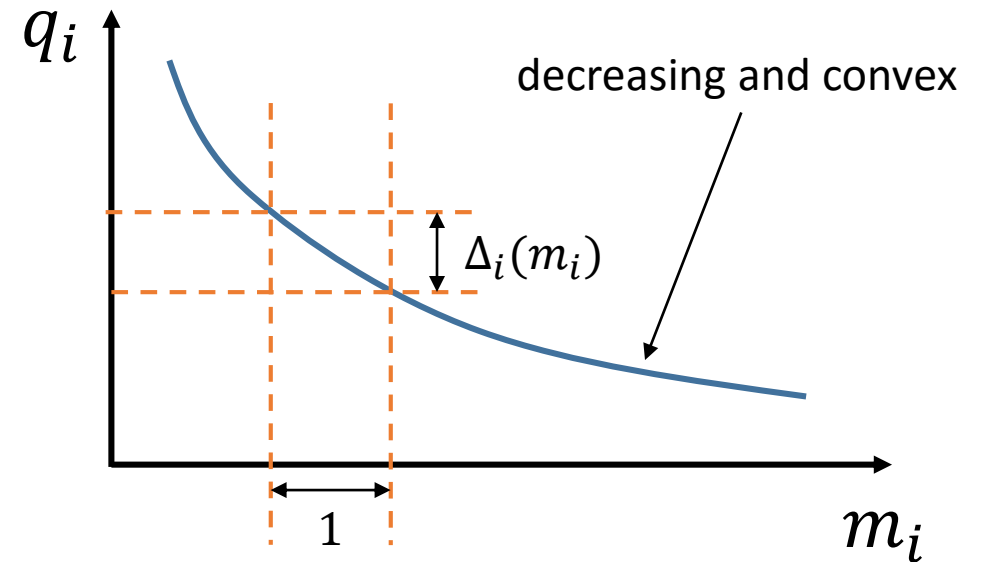
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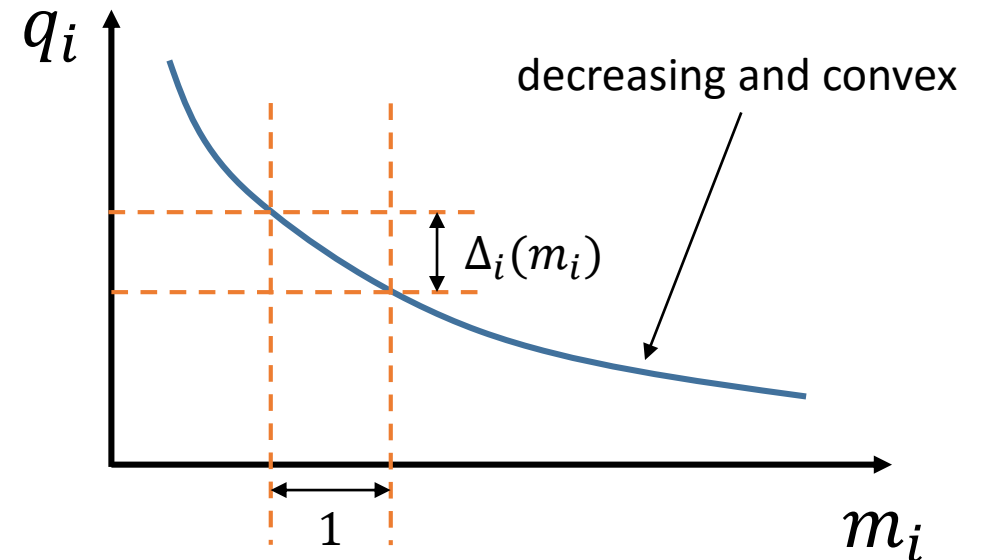
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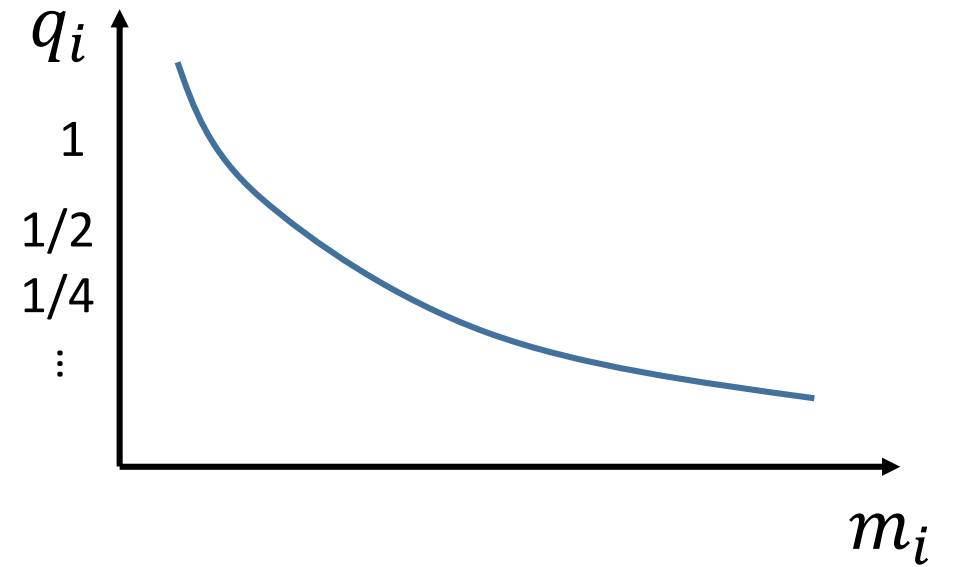
- $$q_i(m_i) = \frac{C_i^m \times m_i}{(D_i - L_i) \times m_i - (C_i^e - L_i)}$$

- $$\Delta_i(m_i) = q_i(m_i) - q_i(m_i + 1)$$

- $$\Delta_i(m_i) > 0 \text{ and } \Delta_i(m_i) > \Delta_i(m_i + 1)$$

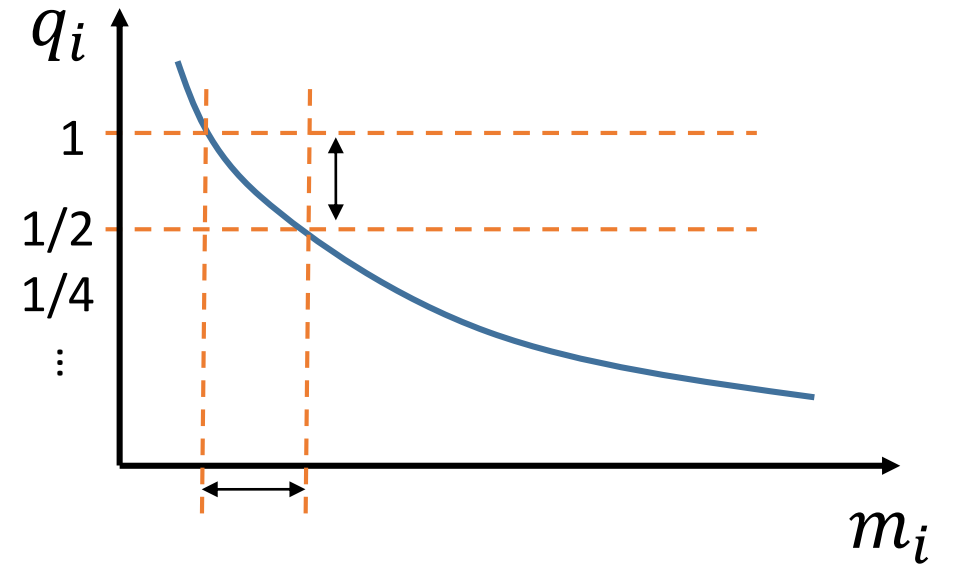


Harmonic RR ($q_i \in \{1/2^j\}$)



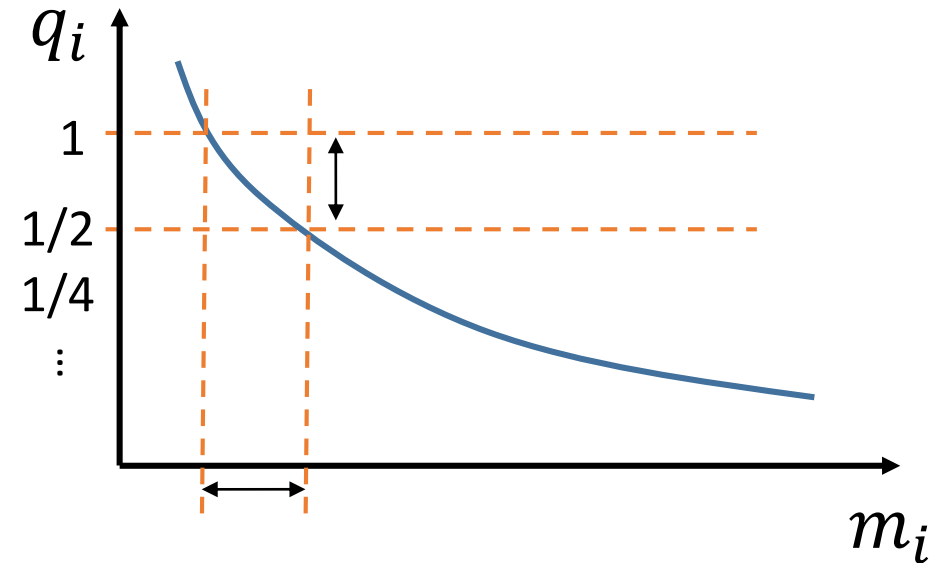
Harmonic RR ($q_i \in \{1/2^j\}$)

- $\Theta_i(q_i) = \frac{q_i - \frac{q_i}{2}}{m_i(\frac{q_i}{2}) - m_i(q_i)}$

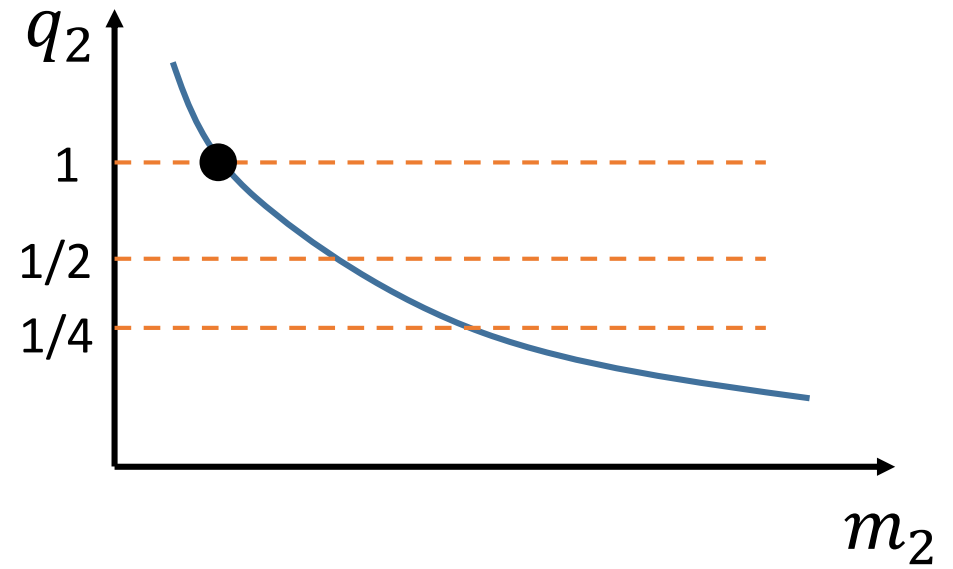
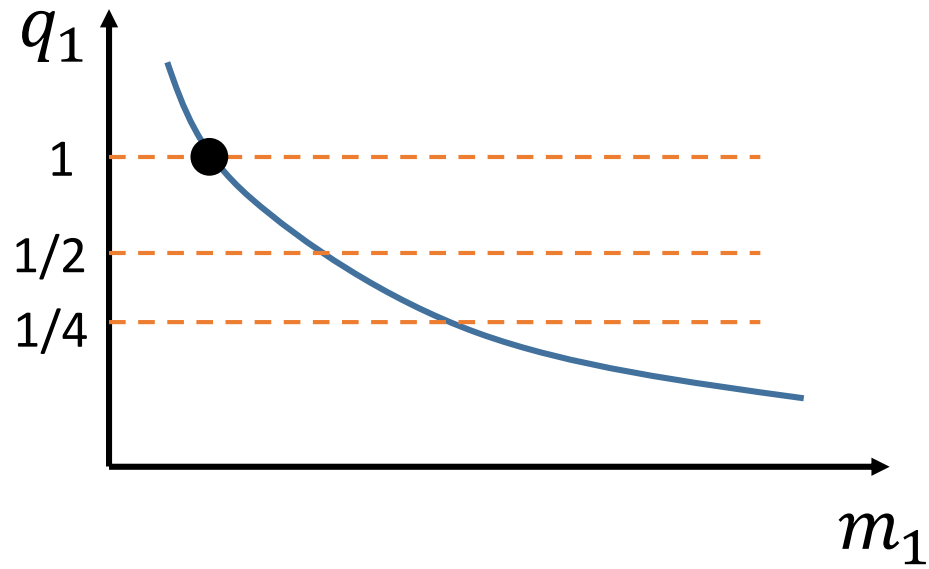


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- $\Theta_i(q_i) = \frac{q_i - \frac{q_i}{2}}{m_i(\frac{q_i}{2}) - m_i(q_i)}$
- We design the algorithm to continue until achieving 100% bandwidth utilization.

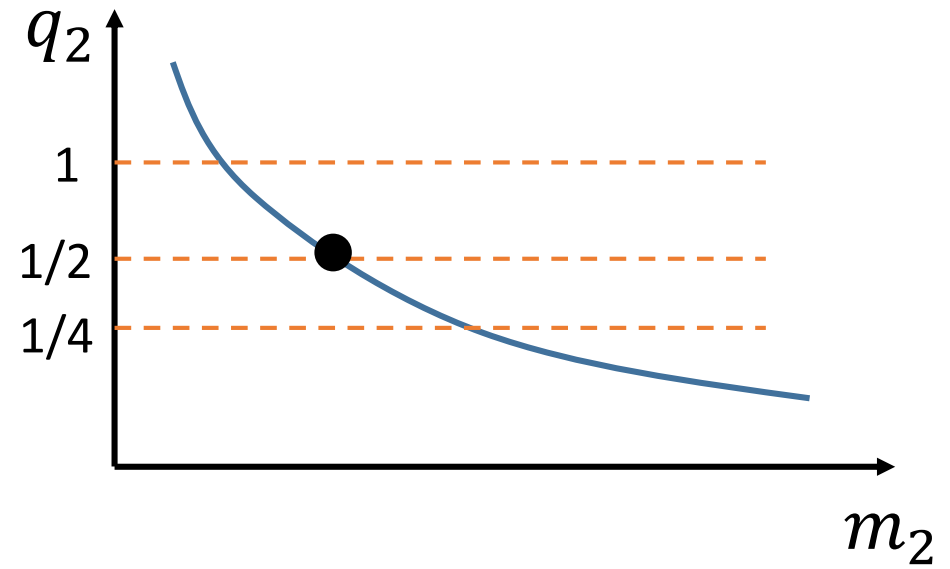
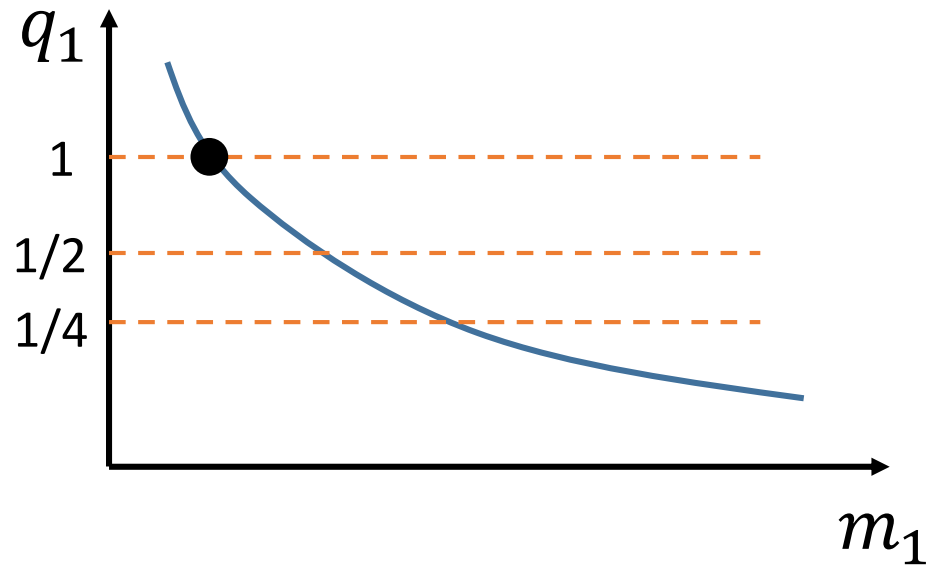


Example



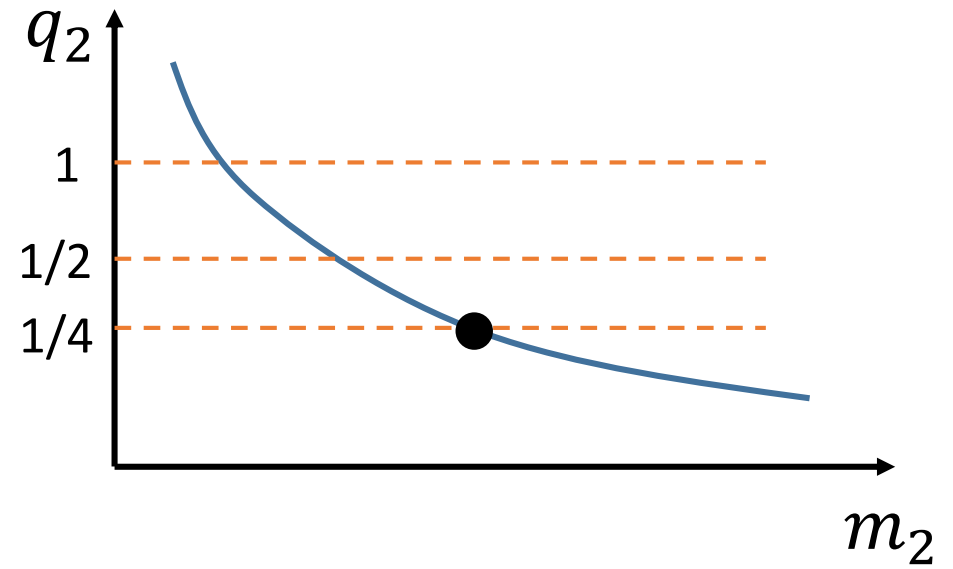
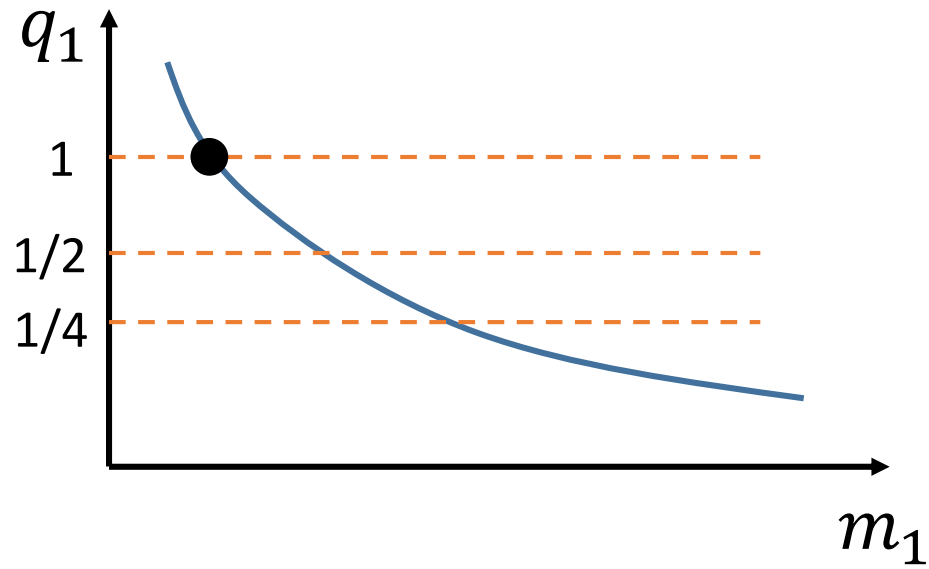
$$q_1 + q_2 = 2$$

Example



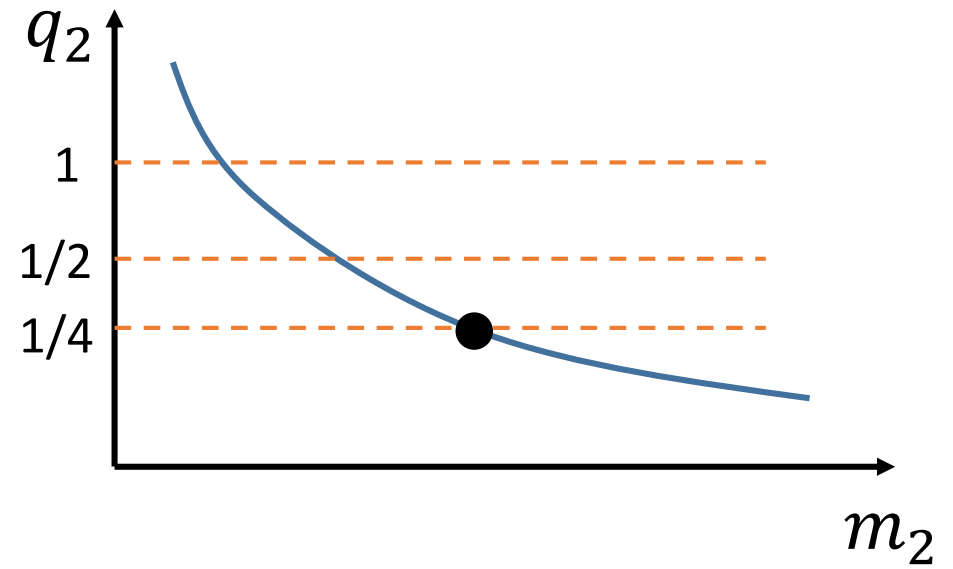
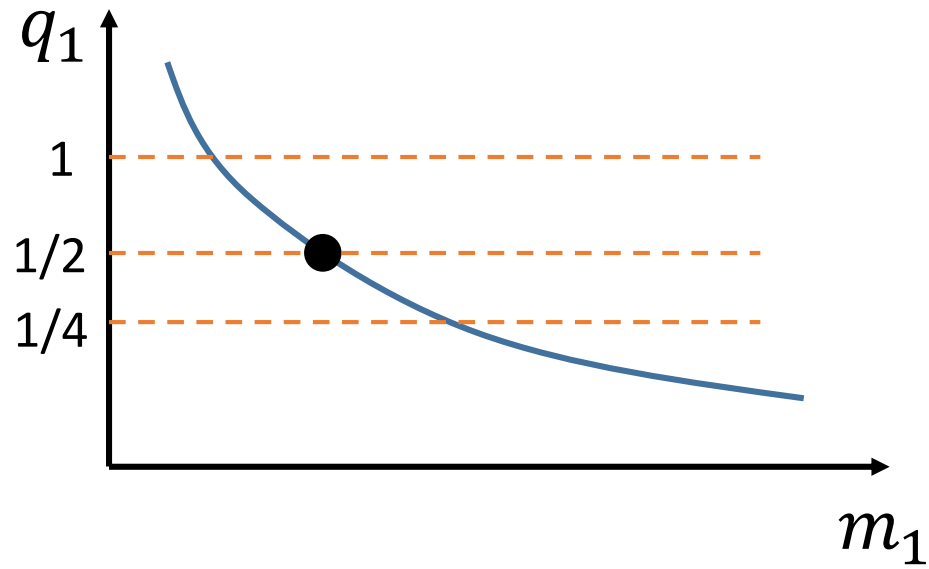
$$q_1 + q_2 = 1.5$$

Example



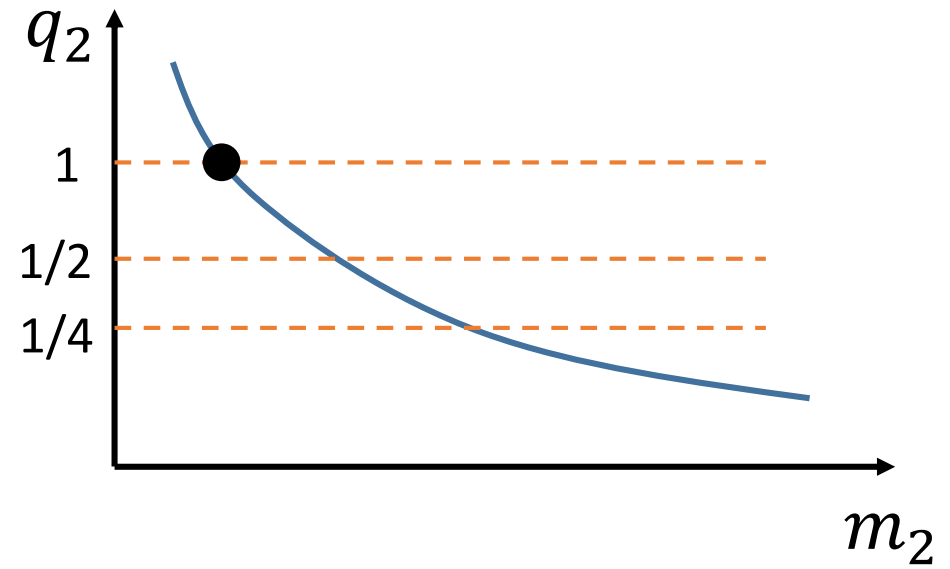
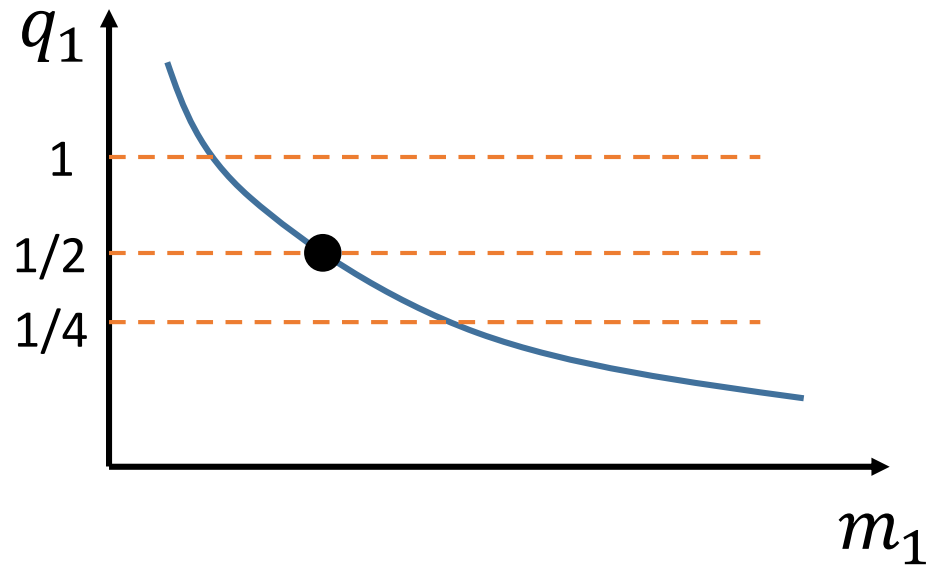
$$q_1 + q_2 = 1.25$$

Example



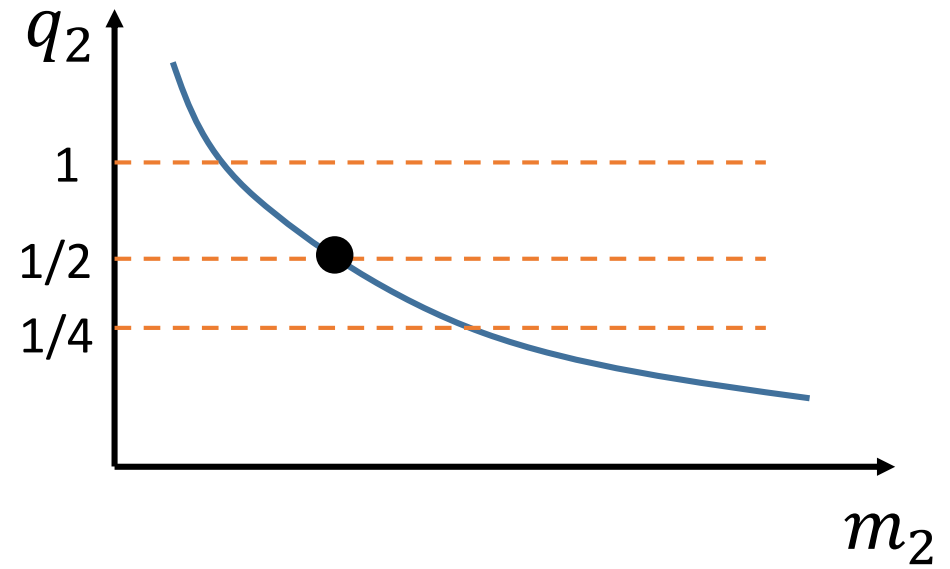
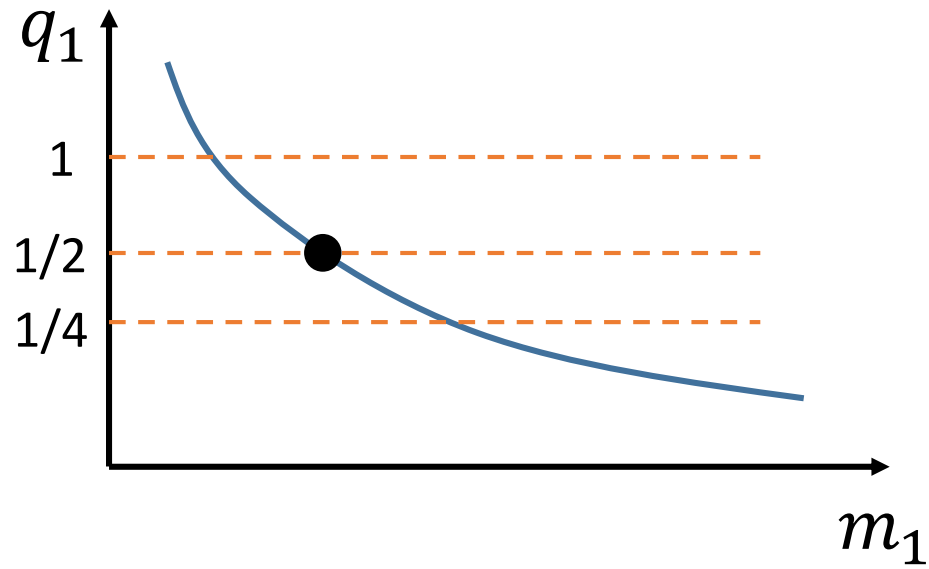
$$q_1 + q_2 = 0.75$$

Example



$$q_1 + q_2 = 1.5$$

Example



$$q_1 + q_2 = 1$$

Memguard

Memguard

- Each task is assigned a budget Q_i

Memguard

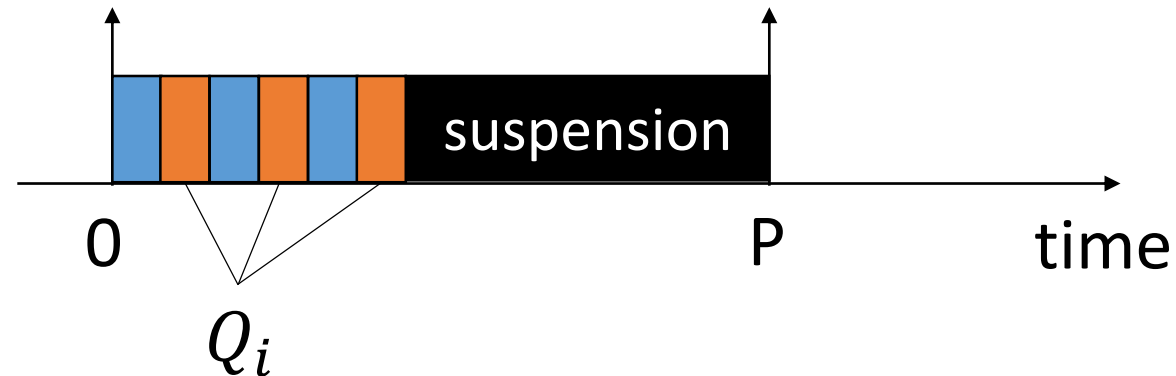
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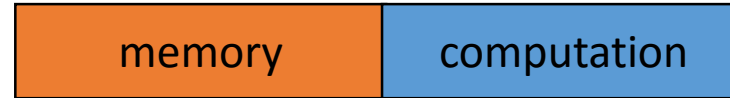
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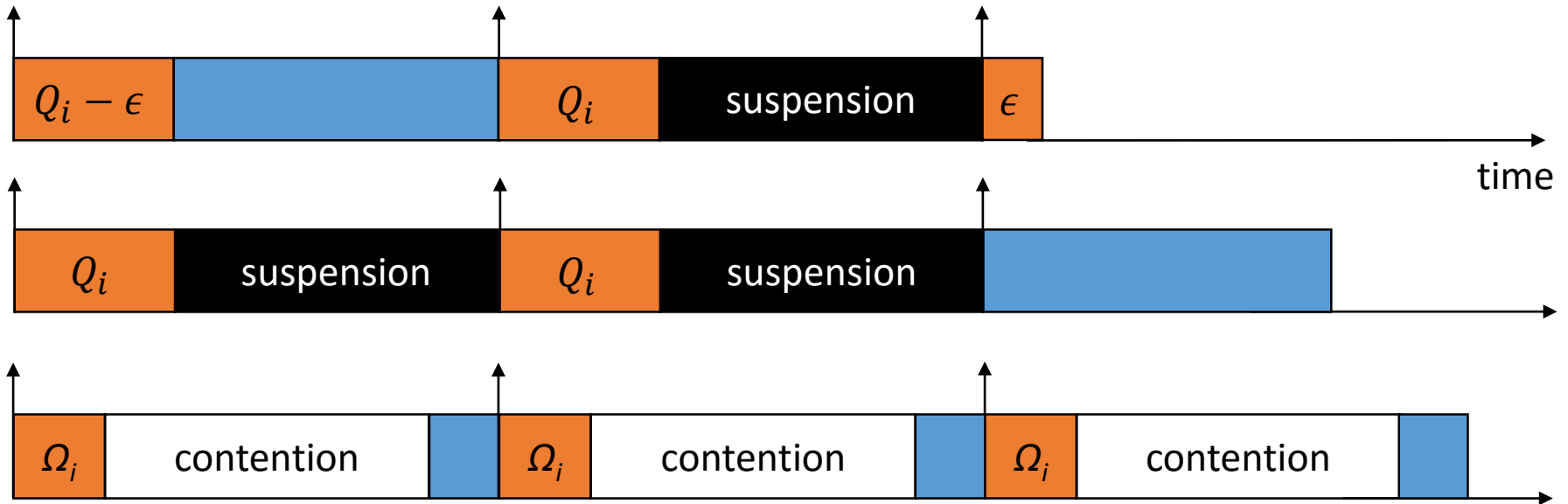
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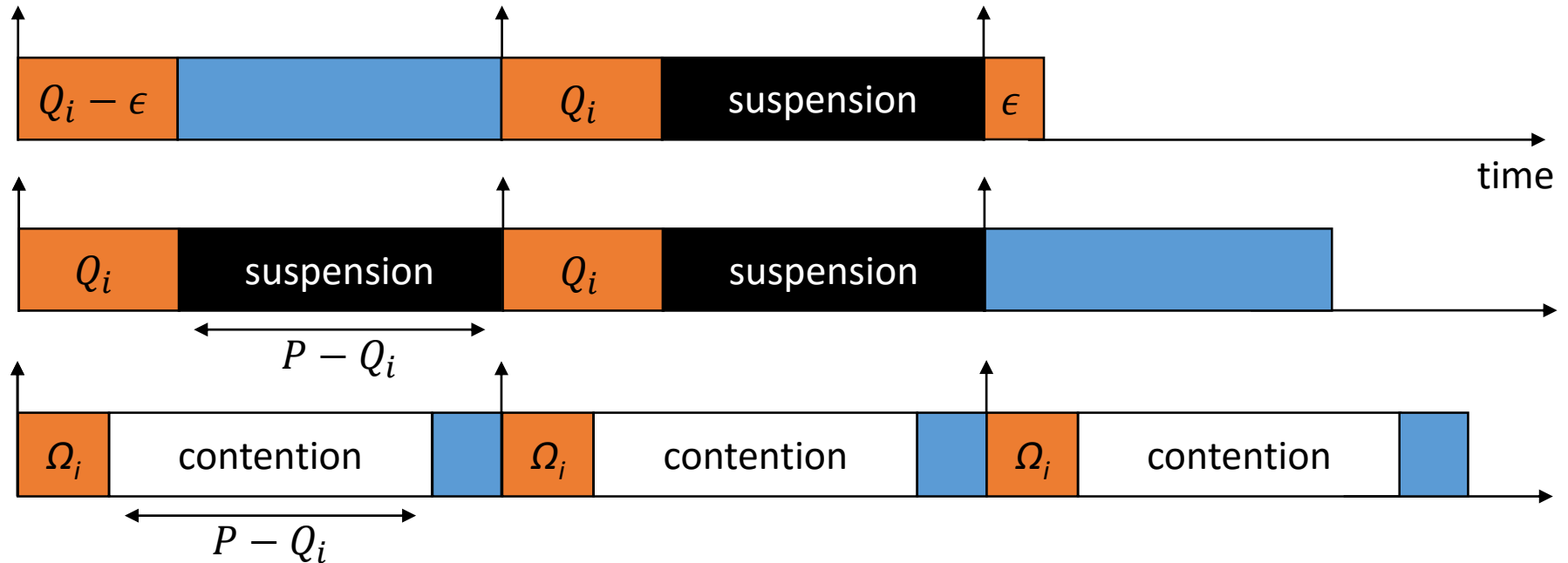
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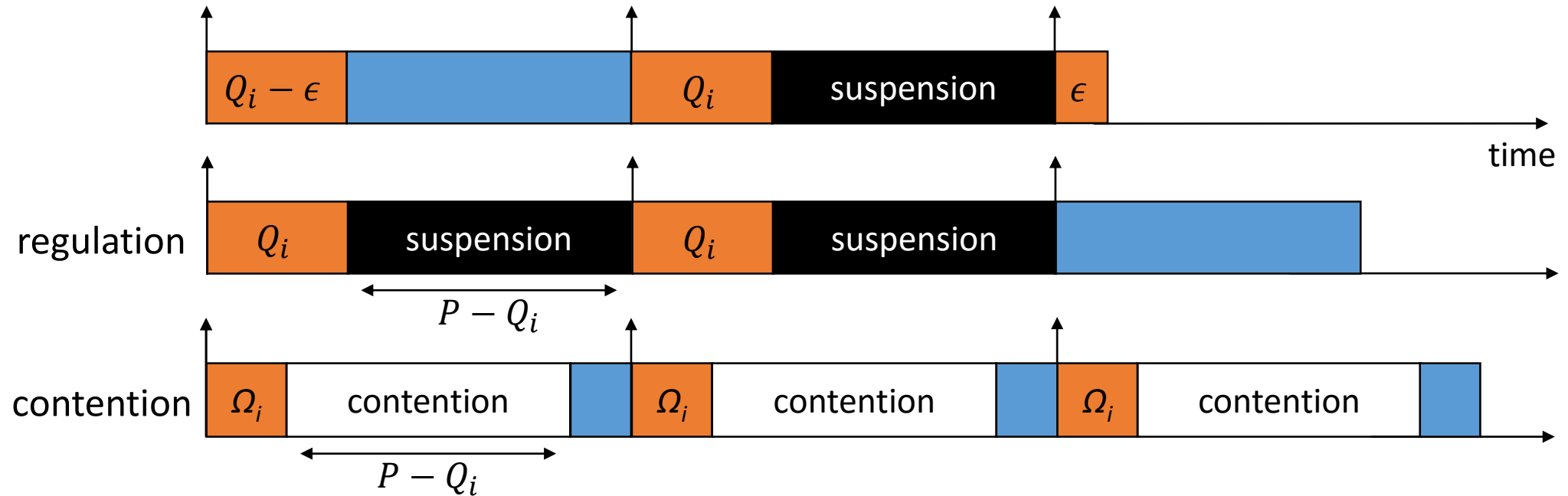
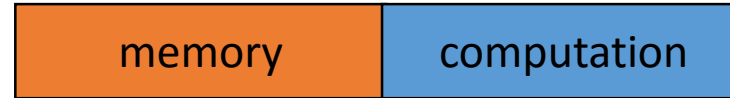
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Memory Time Under Regulation

- $\left[\frac{C_i^m}{Q_i} \right] \times P + P$

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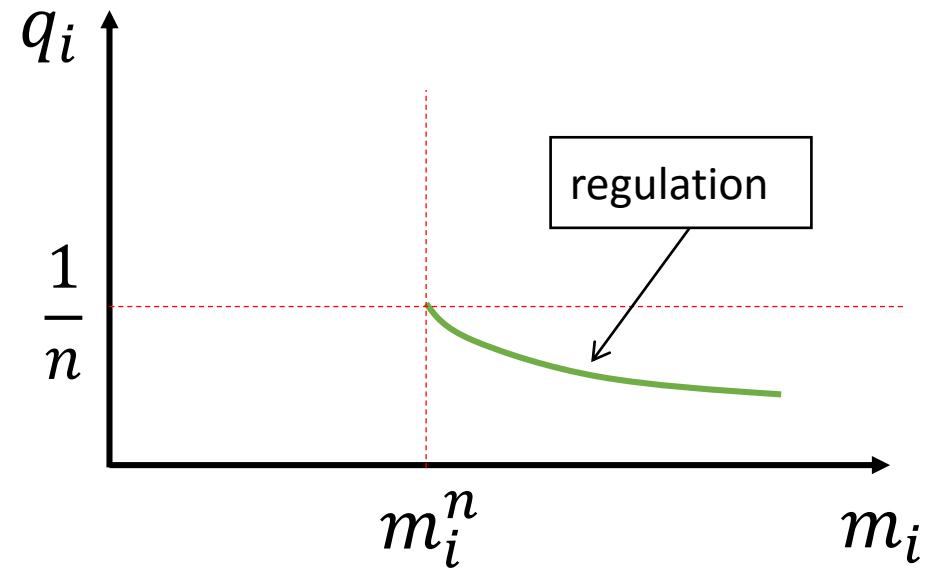
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- $\frac{C_i^m}{q_i} + P$ which is the same as in Optimal-Assign but shifted by constant P

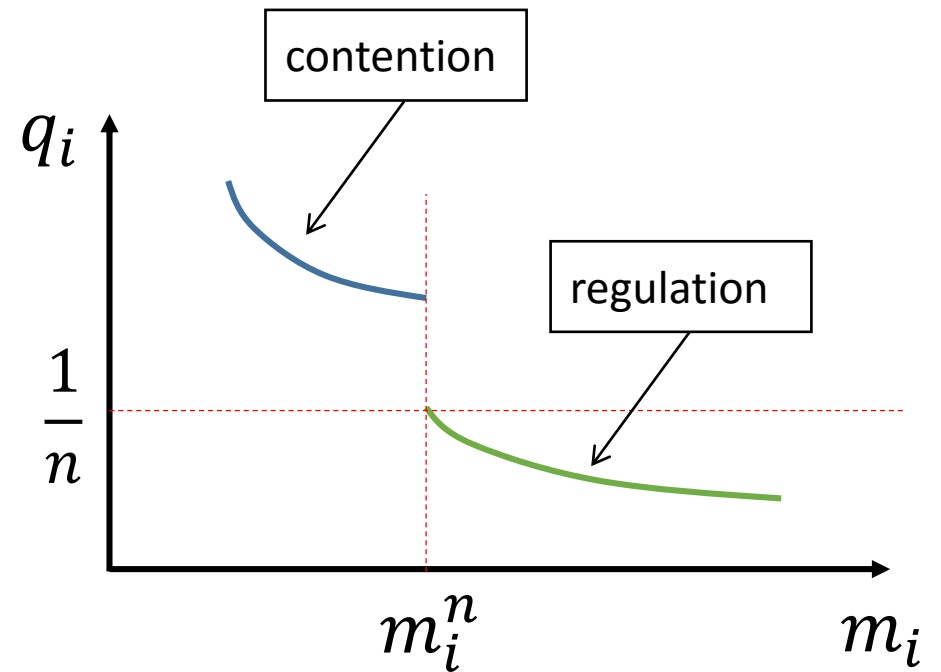
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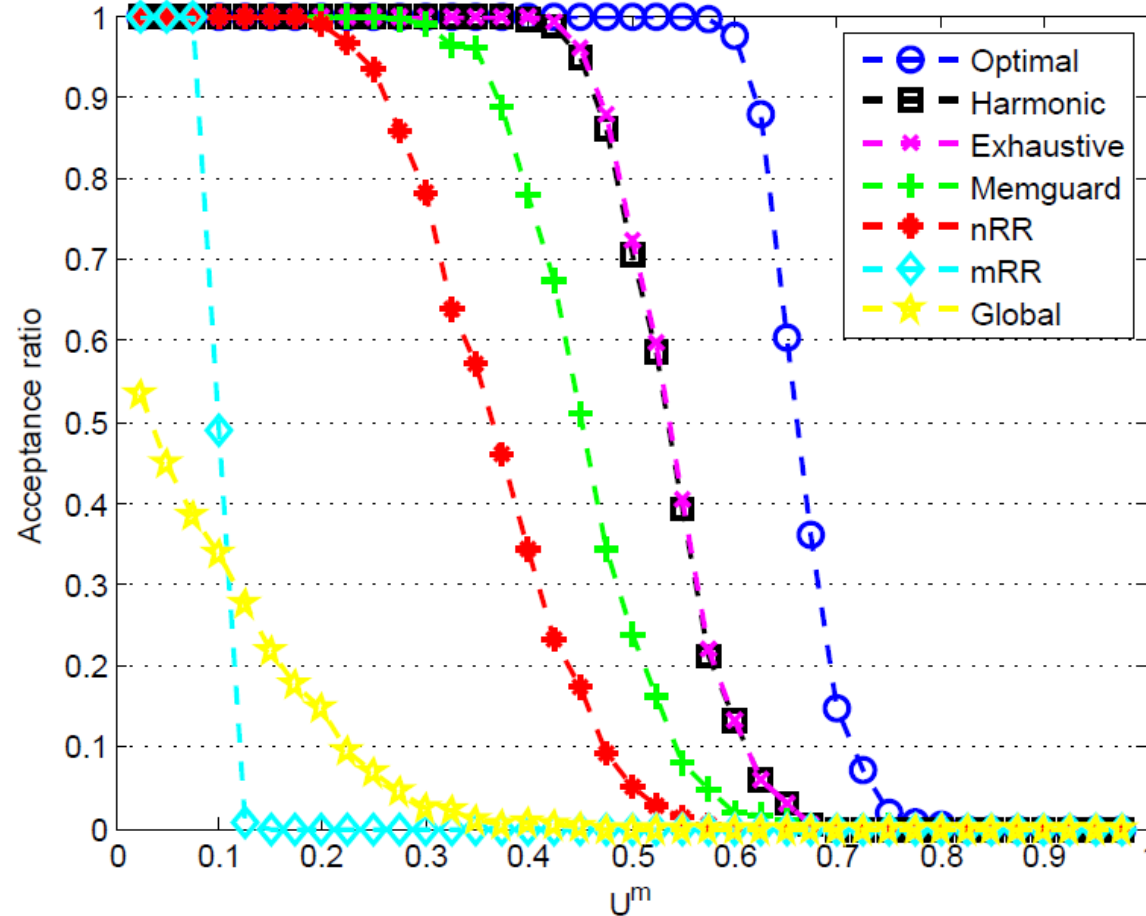
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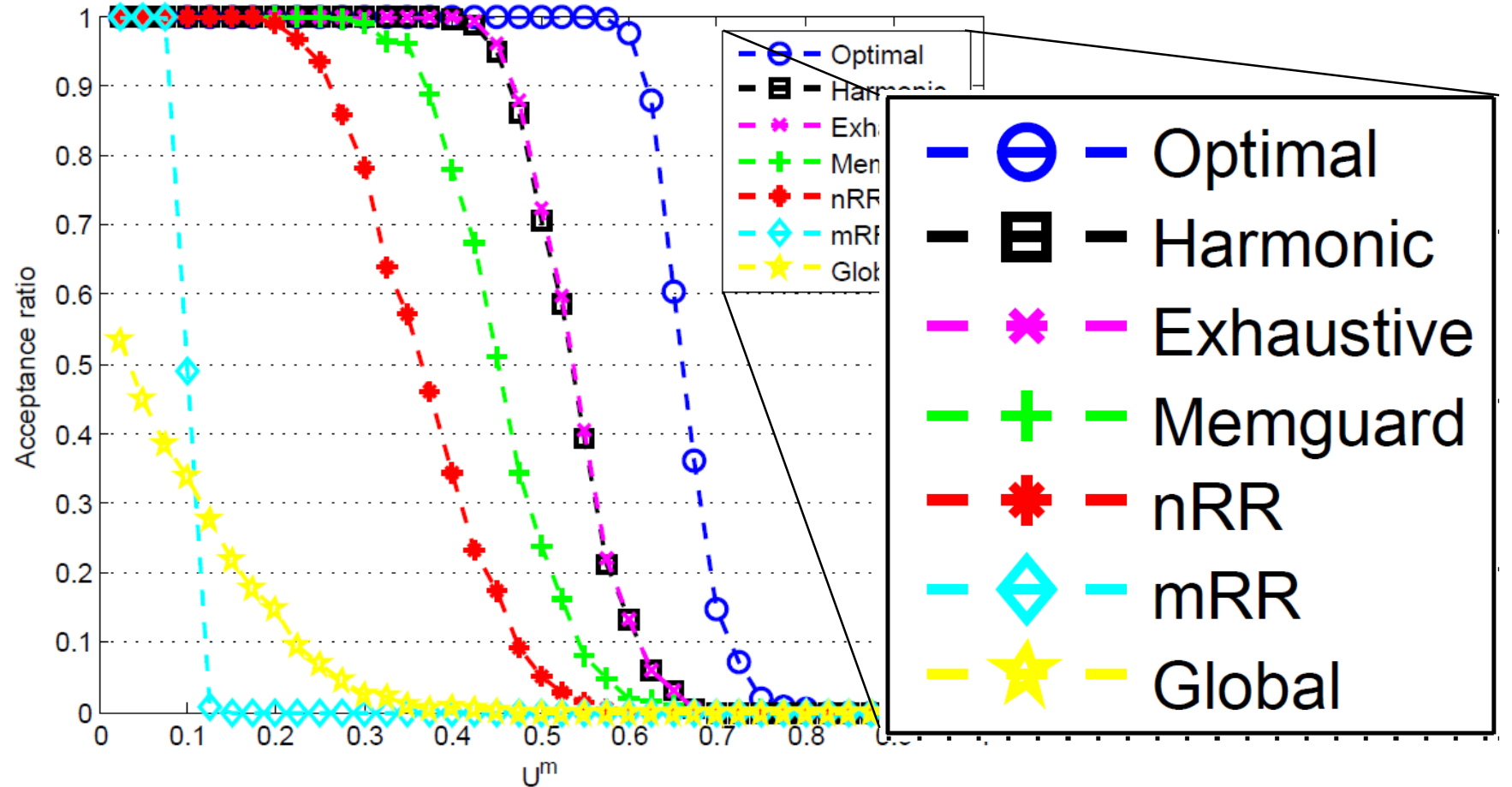
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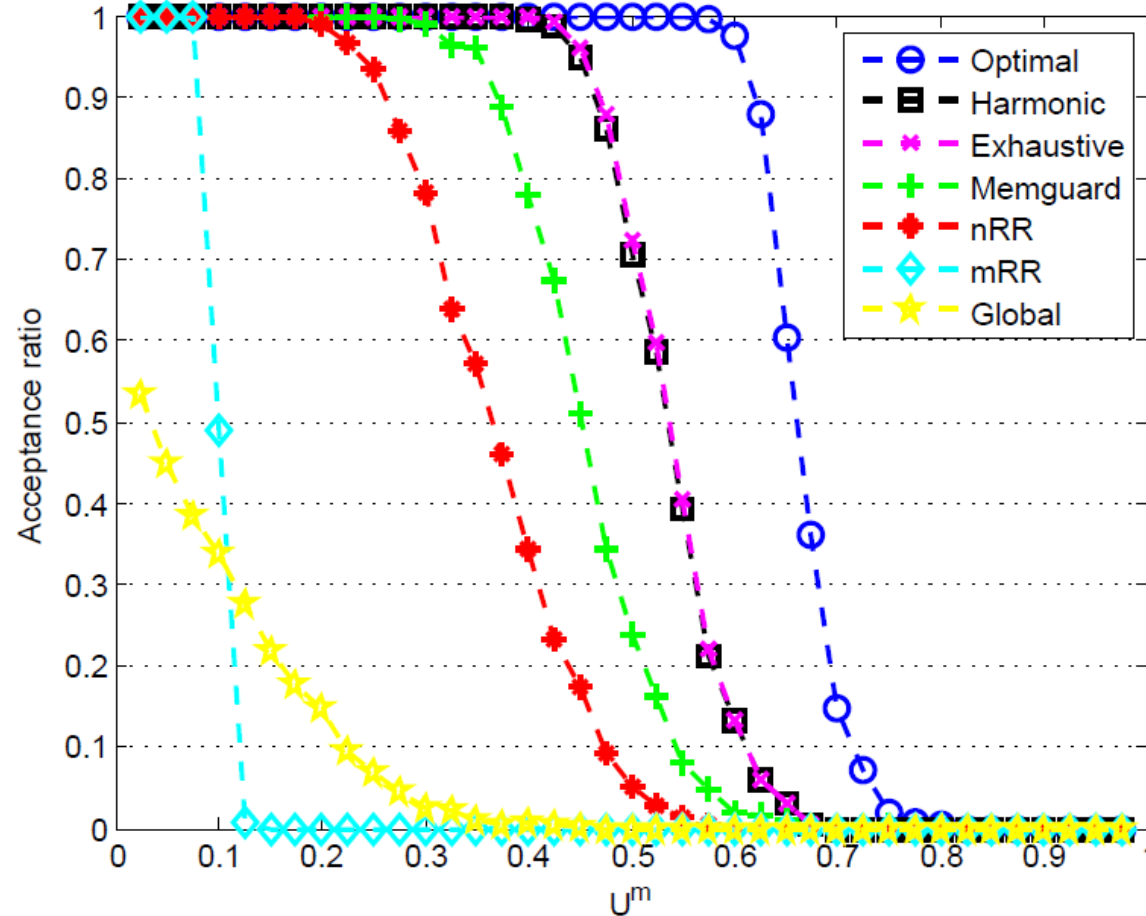
$m = 32, n = 5$ and $U^e = 10$



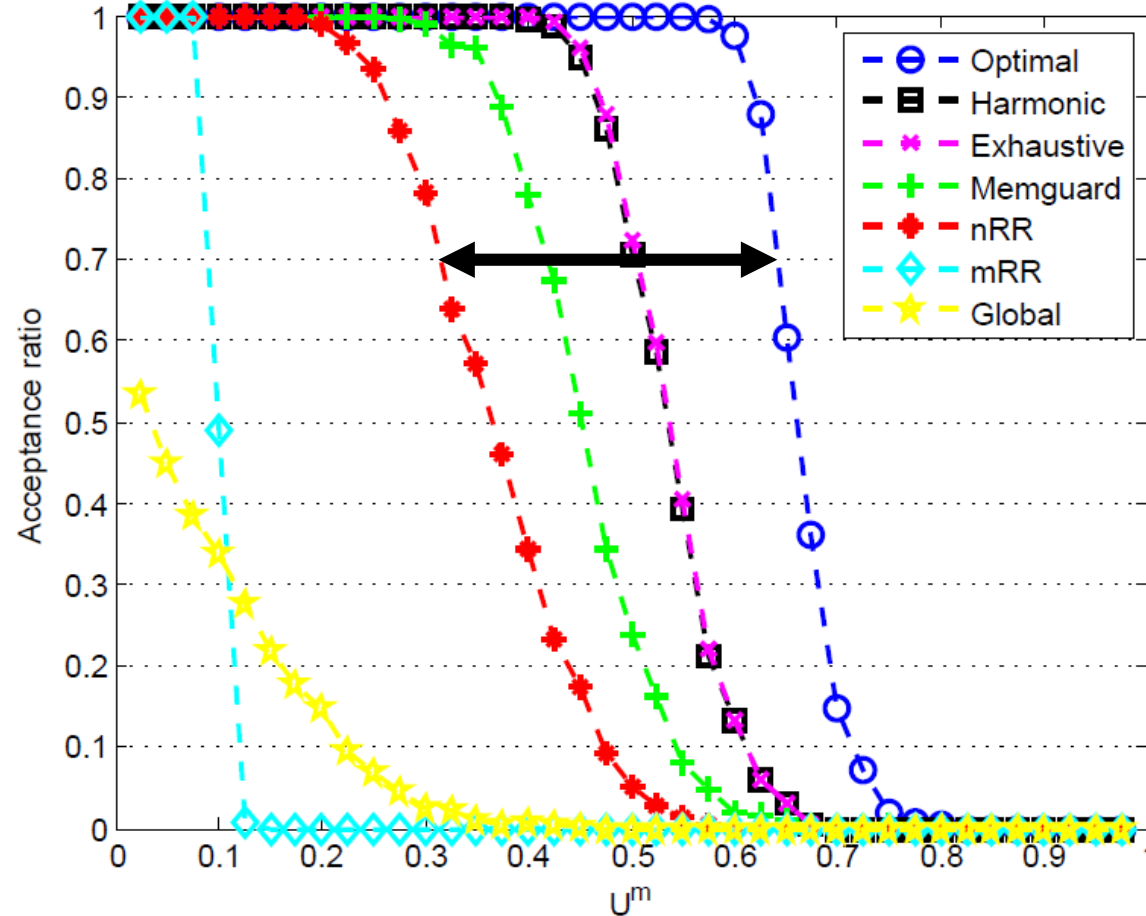
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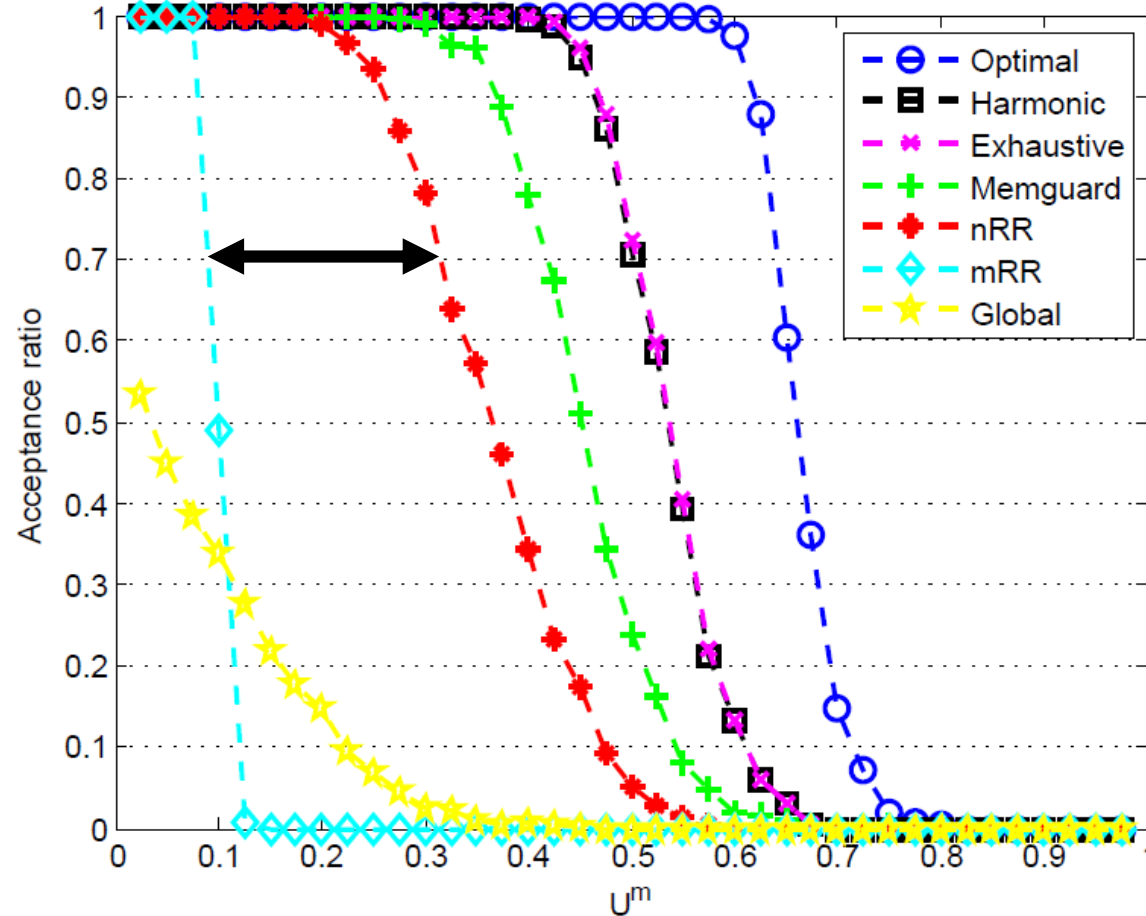
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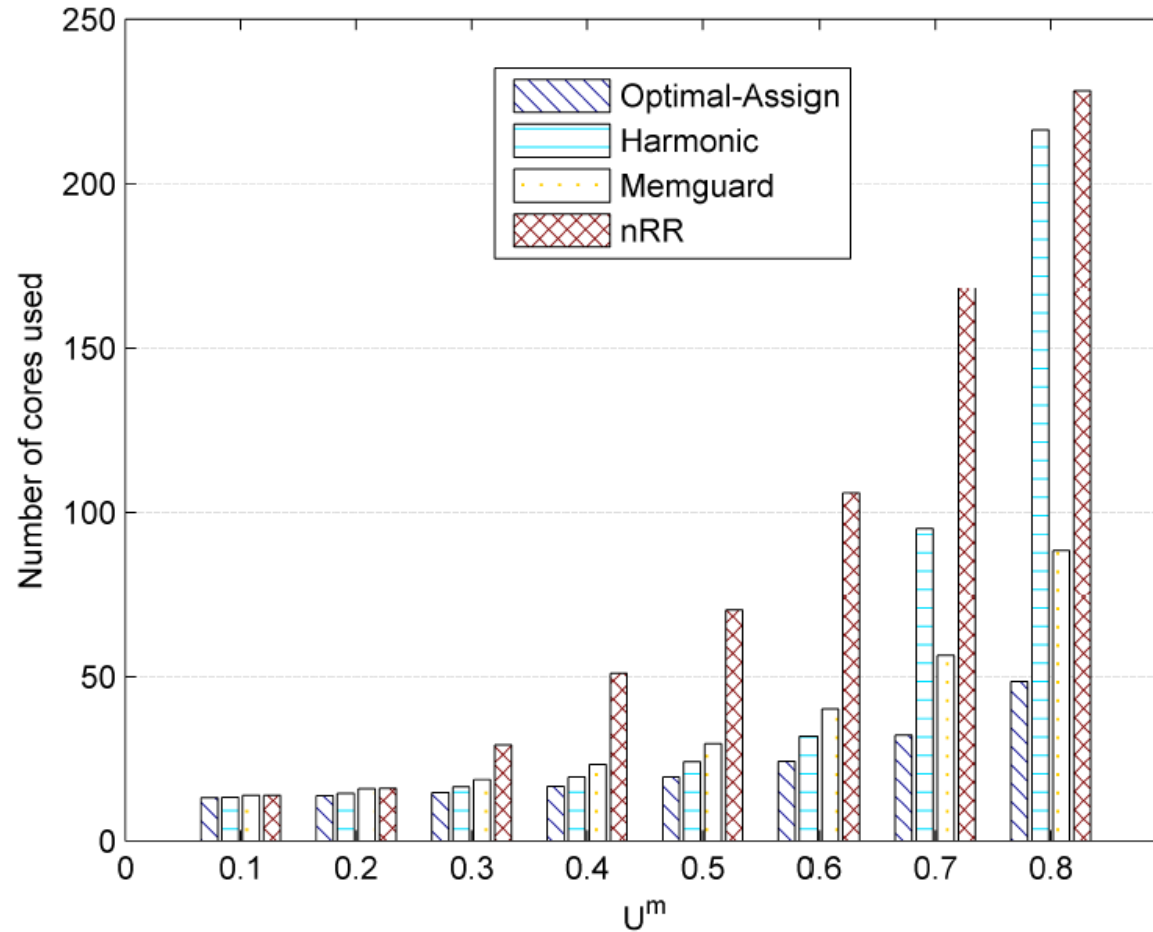
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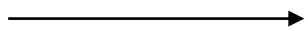
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$m = \infty, n = 5$ and $U^e = 10$



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- In this work, we show how to integrate memory time
- We introduce a novel method to trade cores for memory bandwidth
- We propose three algorithms for this method
- The results indicate a significant improvement over nRR